

Optimizing POL Transient Response with the Tunable Loop™ Feature

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Introduction

Point of Load (POL) DC-DC converter modules are widely used today in a range of applications to provide regulated DC power to a variety of loads. Since POLs are small, efficient and relatively inexpensive, their utility in providing common powering voltages to groups of IC loads has resulted in their rapid adoption and proliferation. With the ever-increasing complexity of today's boards, the number of individual voltages required to properly power all the IC loads ranges from three to ten or even higher. To address this need, architectures that combine isolated DC-DC converters or AC-DC power supplies with POLs have become the new standard.

As the number of board voltages has increased, the ICs have likewise become more demanding. Already at sub-1V and dropping, the new generation of silicon demands ever tighter voltage regulation for optimum performance. This is compounded as designers strive to add more functionality into the same silicon while attempting to maintain the same level of power consumption. The result of lower voltages at the same level of power consumption results in a marked increase in current requirement. An IC that operates at 20W maximum power consumption would draw 11.A at 1.8V, but 16.7A at 1.2V. This is just one challenging implication of the reduction in powering voltage; there are more severe ones to consider.

Challenges in POL Output Regulation

In order to achieve optimum performance, IC manufacturers typically impose tight limits on the input voltage variation that may be tolerated without errors. A common specification is that the voltage may not deviate by more than $\pm 5\%$, and may be as tight as $\pm 3\%$. As the powering voltages drop, these tolerances translate into ever tighter bounds. A $\pm 5\%$ band at 1.8V is 180mV, but at 1V, it is only 100mV.

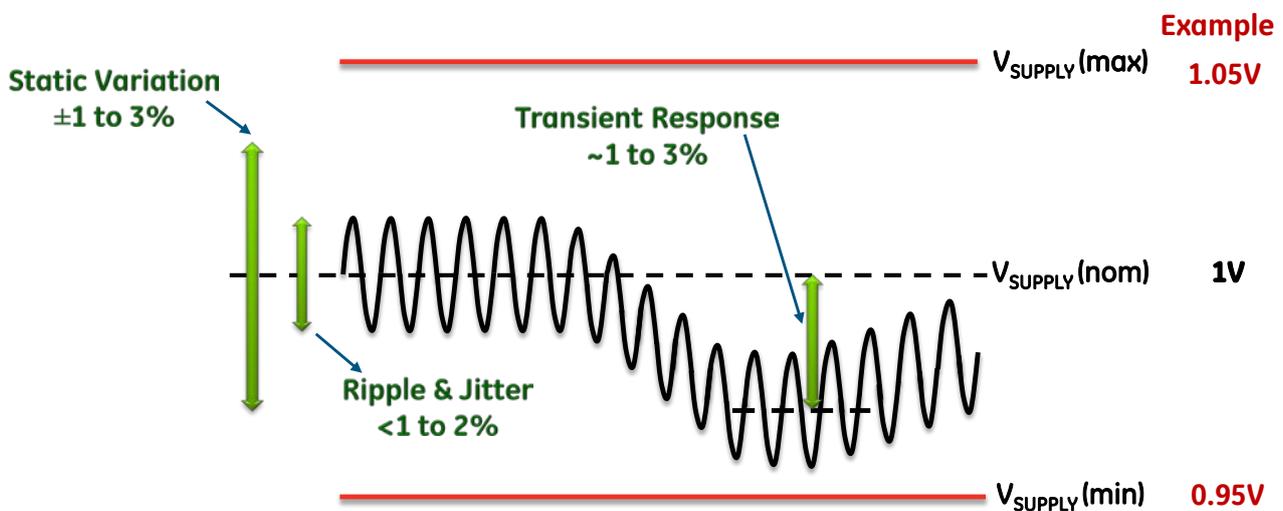


Figure 1. Components of voltage deviation that POLs must address in order to meet IC powering requirements: Static Variation, Ripple and Jitter, and, Transient Response.

The POL powering the IC must maintain this tolerance under varying conditions of input voltage, load current, temperature, component variations, and drift over the life of the product. Figure 1 demonstrates this requirement. The upper and lower bounds for the supply voltage are imposed by the IC being powered. The total deviation is composed of three elements: (1) static deviations (variation of the POL average voltage due to component tolerances, temperature, line, and load regulation), (2) POL switching output ripple, and (3) dynamic voltage variations due to transient load changes.

Typically a budgeting process can be used to allocate the entire allowed voltage deviation window among various contributing factors. For example, out of a total band of 10% of the nominal powering voltage, the worst case static deviation may be 3%, output ripple may be 1% and with a 2% safety margin, this would leave 4% for transient

deviation. The actual transient deviation then allowed for a minimum to maximum load current change would then be half of the 4% or 2%. At 1.8V this translates to 36mV, at 1V it drops to 20mV. Referring back to the current draw on a 20W load, a 50% transient load change at 1.8V translates to 5.6A, but at 1V, it becomes 10A.

Power Draw	IC Voltage	Current	Regulation Band ±5%	Transient Band 2%	50% Load Step
20W	1.8V	11.1A	180mV	36mV	5.6A
20W	1V	20A	100mV	20mV	10A

As powering voltages drop, the voltage deviation tolerance shrinks while the load step increases. This compounding impact results in a problem that is thrice as difficult (1.8X higher current step / 0.6X specified deviation band).

Historically, the solution to improving the transient response of POLs has been to increase the capacitance between the POL module and the IC. The additional energy storage provided by the capacitors reduces the deviation in the output voltage during a transient load step. The implications, however, are increased cost, increased board area, and reduced reliability. Furthermore, this brute-force solution eventually runs out of steam and begins to degrade the transient response causing an increasingly sluggish recovery time. Finally, this approach hits a hard limit where adding more capacitance results in a low margin of stability and eventually the full onset of instability.

The Tunable Loop™ Feature

The traditional solution to improving the transient response by adding more capacitance is illustrated in Figures 2a and 2b. The response of a GE 12A PicoDLynx™ POL module at 1.2V out with a 50% load step (6 Amps) is presented using a single 47µF capacitor and 47µF + 330µF capacitors. Clearly, there is an improvement, but it falls far short of optimizing the response to the load transient. The Tunable Loop™ feature [1] patented by GE provides the answer. Figure 3c demonstrates the substantial improvement afforded through the implementation on the Tunable Loop. Clearly, with an ever-tightening budget of voltage deviation, and an ever increasing load step demand, the immediate impact of this technology is apparent.

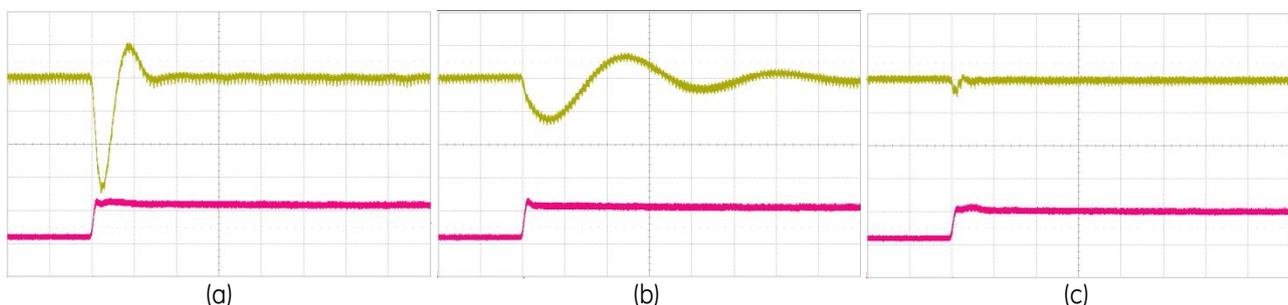


Figure 2. Waveforms of output voltage (upper) and current (lower), showing how transient response is improved by adding external capacitors and the Tunable Loop™. For all plots the output voltage scale is 100mV/div., the load current waveform scale is 5A/div., and the time scale is 20µs/div.

The output voltage response by POLs is a function of two parameters: (1) the external capacitance and (2) the control bandwidth of the POL+load. Figure 3 illustrates the role of external capacitance in reducing the output voltage deviation due a transient load change. Due to the POL's limited bandwidth (typically the control loop gain crosses through the 0dB point at no more than 1/10th of the switching frequency), the initial surge of current is provided by the external capacitors. Once the POL control loop is able to come into play, the new level of load current is provided by the POL and the current from the external capacitor goes to nearly zero. Hence external capacitors improve transient voltage response by providing additional energy during the transitions between load current levels. As external capacitance is added, the initial deviation due to a load transient is reduced further, leading to the conclusion that lower transient voltage deviations are achieved simply by adding more capacitance.

The POL control bandwidth is the other parameter that controls transient deviation. Figure 4 illustrates that as the control bandwidth increases; the transient response improves for a fixed external capacitance. Consequently, it can be seen that as long as stability is maintained, increasing control bandwidth continues to improve transient response.

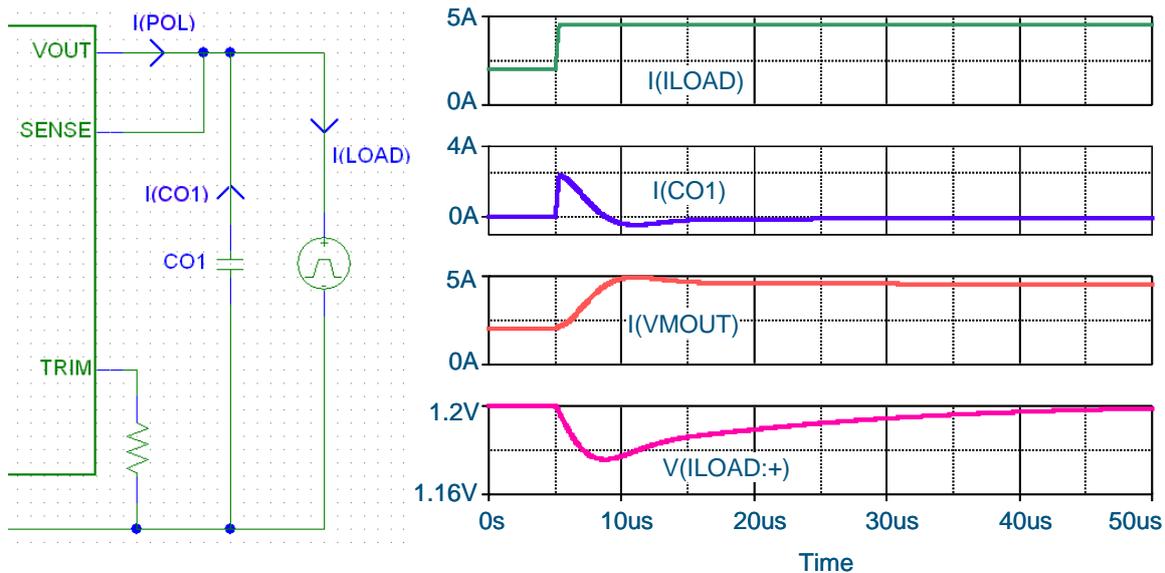


Figure 3. Diagram and waveforms explaining the role of output capacitance in helping a POL DC-DC converter reduce output voltage deviation due to a transient load change.

While increasing control bandwidth and increasing the external capacitance both improve transient response, these parameters are not independent. In fact, there is a strong interaction between them as increasing the external capacitance degrades the control bandwidth of the system. Therefore, the full benefits of the external capacitance cannot be realized unless this degradation is counteracted. This is the function of the Tunable Loop feature. It allows the designer to re-tune the control loop to compensate for the additional external capacitance resulting in an optimum balance of capacitance and bandwidth yielding the best transient response possible for a given set of application requirements.

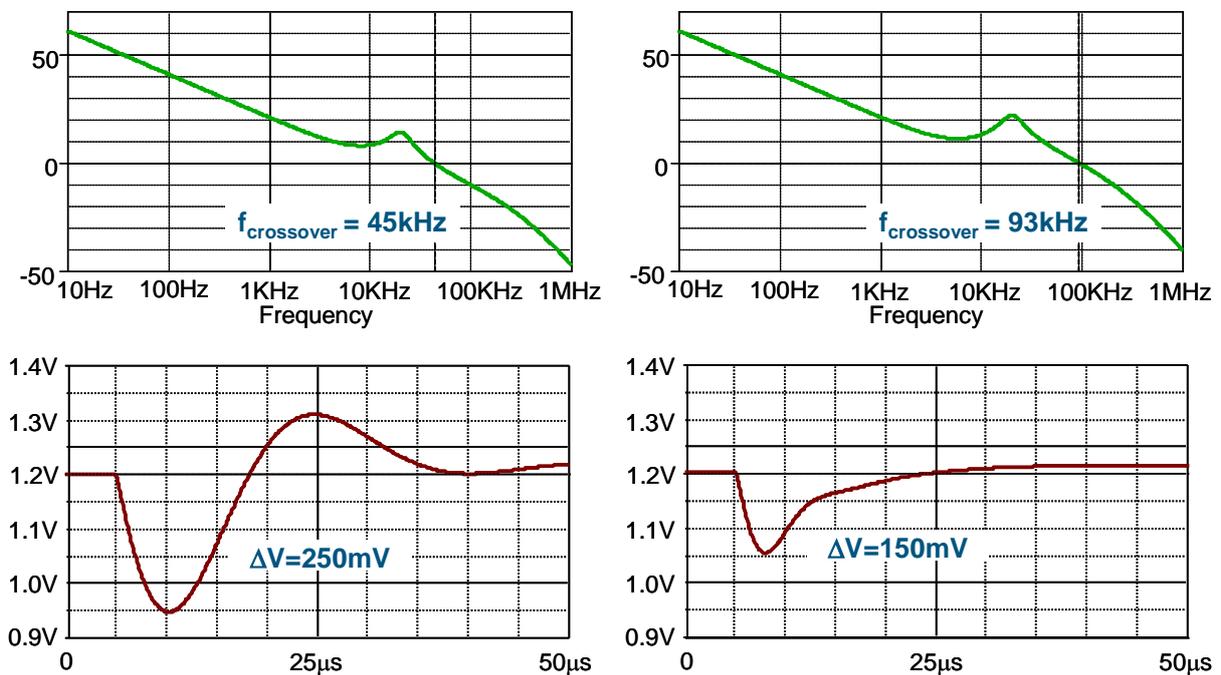


Figure 4. Plots showing the effect of improved control bandwidth on output transient voltage response. Output capacitance is the same in both plots.

The power of the Tunable Loop™ is in its simple implementation. As shown in Figure 5, an external network consisting of a resistor and capacitor in series is connected across the TRIM and Vout (or SENSE) pins of the POL module. These are typically very small, inexpensive passive devices: The resistor may an 0805, 0603, or 0402 SMT component ranging in resistance from a few Ω to a few k Ω . Likewise, the capacitor is similar in size ranging from a few hundred pF to a few hundred nF. Fundamentally, this allows a single POL module to be externally optimized across multiple

applications of significantly varying demands with minimal effort yielding the optimum board area, cost, response, and reliability. This additional benefit of module consolidation through a simple programmable feature yields significant dividends on both technical and commercial levels.

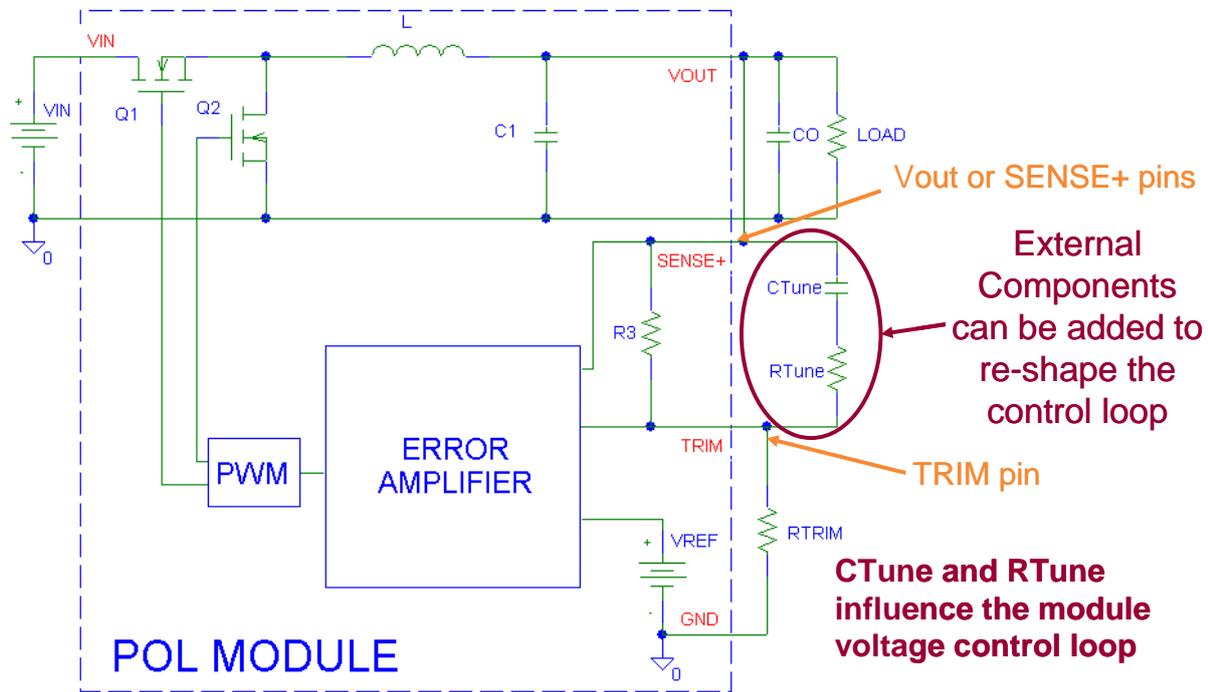


Figure 5. Diagram showing how the Tunable Loop™ feature can be implemented by adding two inexpensive components CTune and RTune to re-shape the POL voltage control loop.

Example Converter with the Tunable Loop™ Feature

Let us consider the example of a 12A PicoDLynx™ converter. Through simulation models, we can easily examine both the transient response and control loop behavior. First, let's consider the impact of adding more capacitance. Figure 6 illustrates the transient response of the converter to a 50% (6 Amp) load step at different levels of external capacitance (1x47µF, 2x47µF, 3x47µF and 4x47µF). Note that while the maximum voltage deviation does improve from 347mV (1x47µF) to 222mV (4x47µF), the control loop bandwidth drops from 51kHz to 24kHz. This can also be noted in the increased sluggishness of the voltage recovery so that while adding capacitance does reduce the peak voltage deviation, it simultaneously increases the duration of the voltage excursion. This is consistent with the reduction in control bandwidth and poorer phase margin by the increasing capacitance.

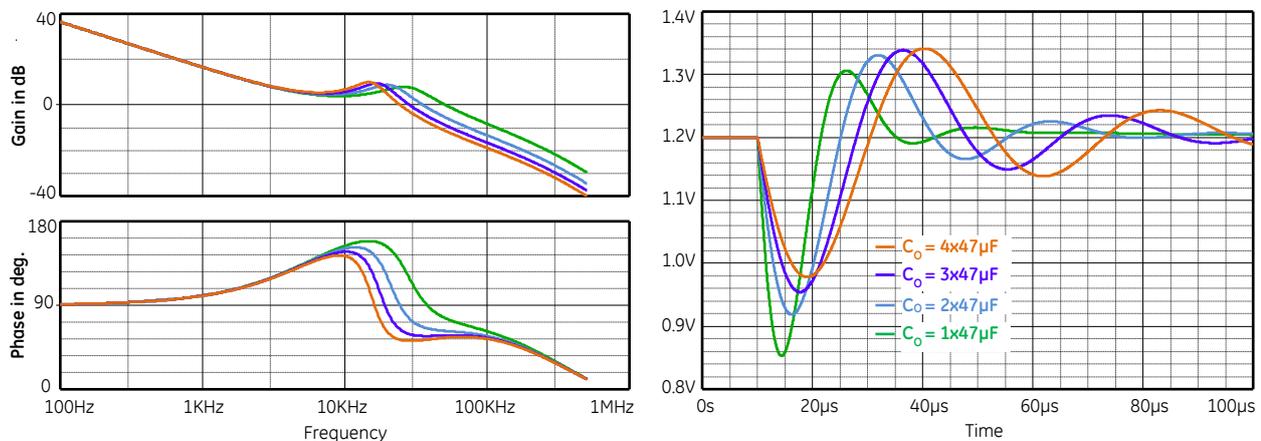


Figure 6. Plots showing the effects of adding external capacitance to a 12APicoDLynx™ module. The plots on the left show the loop gain plots while the waveforms on the right show the output voltage transient response to a 6A step change in load current.

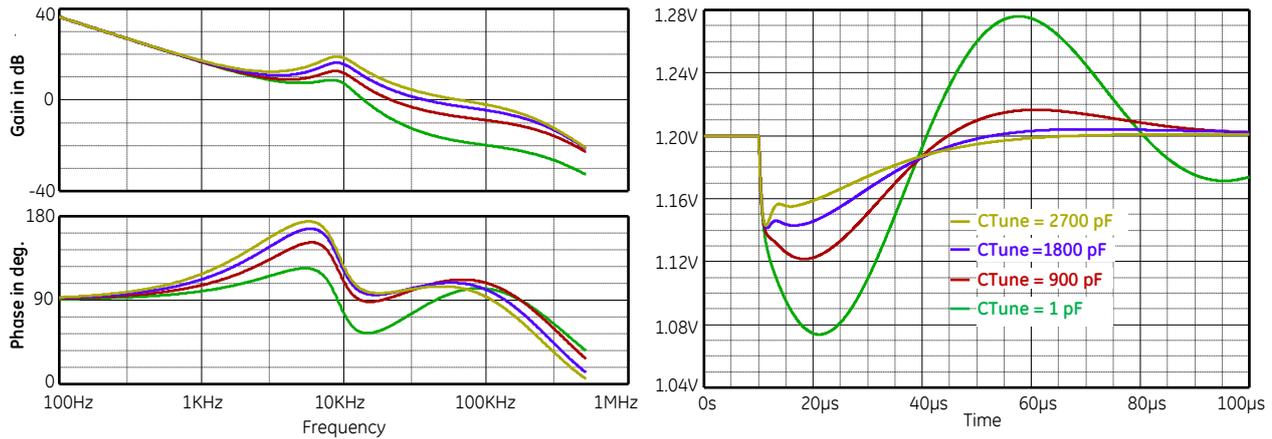


Figure 7. Plots showing the effects of externally tuning the compensation of the 12A PicoDLynx™ module with external capacitance of (1x47μF + 1x330 μF) using the Tunable Loop™. The plots on the left show the loop gain plots while the waveforms on the right show the output voltage transient response to a 6A step change in load current.

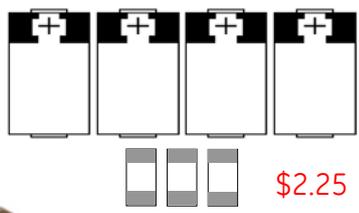
The ultimate goal is to regain the bandwidth lost due to the increased capacitance through the use of the Tunable Loop™ feature. To demonstrate the process, we fix the value of RTune to 330Ω and vary CTune from 1pF to 2700pF. Figure 7 illustrates increasing CTune correspondingly increases the control bandwidth from 13.7kHz (CTune=1pF) to 64.5kHz (CTune=2700pF). The Tunable Loop has recovered and even exceeded the lost bandwidth, but the true benefit is evident as the voltage deviation improves from 126mV to 57mV. Note that the voltage waveform also settles much faster and without overshoot. Here, the Tunable Loop achieves a 2.2x voltage deviation reduction at the same level of capacitance.

Alternately, the Tunable Loop can achieve a lower voltage deviation specification with a significantly reduced capacitance. Figure 8 graphically demonstrates the size and cost reductions obtained by using the Tunable Loop for another example design using the 12A PicoDLynx™ module to power an application from 5Vin to 1.2Vout @ 8A, with a maximum step load of 4A and with a required output voltage deviation to not exceed 4% (48mV). For the case where the Tunable Loop™ is not used, 3 x 47 μF ceramic and 4 x 330 μF polymer electrolytic capacitors are required, whereas when the Tunable Loop™ is employed, only one each of the 47μF and 330μF capacitors are needed. This results in a \$1.45 reduction in external capacitor cost and a drop in PWB space needed of 190 mm² (0.3 in²). Since the module itself occupies only 149 mm², the total board area reduction is very significant.

- **No Tunable Loop**
 - 3 x 330μF Sanyo 4TPF330ML (330μF/40mΩ)
 - Board area of 258 mm² (0.4 in²)
- **With Tunable Loop**
 - 3 x 47μF ceramic (1206 size)
 - Board area of 67.6 mm² (0.105 in²)

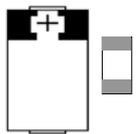


Caps: No-Tune



\$2.25

Caps: Tune



\$0.60

Figure 8. Size and cost reductions derived from using the Tunable Loop™ on an example design employing the 12A PicoDLynx™ module.

Greater reductions in cost and board area due to external capacitance can be achieved with higher current modules. Figure 9 shows graphs of output capacitance vs. output voltage deviation for a 40A module where a 10A step load is applied. In addition to the reduction in output capacitance that the Tunable Loop™ provides, the range of external capacitance that can be attached to the module is about 6X larger than without tuning. This powerful capability also

enables the use of much larger values of external capacitance with POLs when either very low values of output ripple are needed or extremely small transient voltage deviations are required.

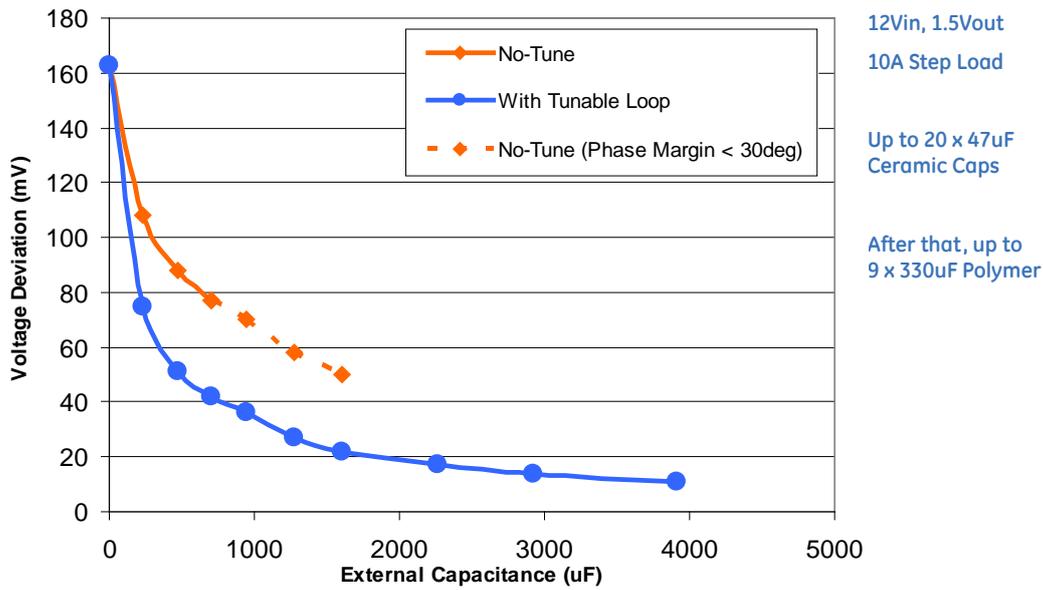


Figure 9. Graph showing output voltage deviation due to a transient load current of 10A vs. external capacitance for the case of a 40A module with and without the Tunable Loop™.

While the cost and board area savings are significant, another benefit of using fewer capacitors, and potentially only ceramic capacitors, is higher reliability. Additionally, the simple tools made available in the configuration of the Tunable Loop parameters lead to better characterized and more robust designs with a higher likelihood of getting it “right the first time”. Where design parameters are susceptible to change, stability characteristics can likewise change. An example of this is capacitor ESR variations due to variability in procurement. Having the flexibility to change and tune the dynamic characteristics of the design via the Tunable Loop™ components provides a powerful level of robustness.

Summary

The Tunable Loop™ is shown to be a powerful technique that helps designers optimize the amount of external capacitance needed when employing standard POL modules. Reducing capacitors leads to lower cost, more compact designs and better reliability. GE now offers the Tunable Loop™ on a wide range of POLs, the DLynx™ and TLynx™ series of SMT modules and the Naos Raptor™ series of SIP modules covering output current ranges from 2A to 60A. The data sheets of these modules provide an initial set of recommended values of CTune and RTune for a range of applications. Simulation models and selection tools for all converters that support a wider range of optimization choices are also available and these provide additional benefits in being able to predict design performance before committing to hardware. The flexibility of Tunable Loop™ modules allows for a significant consolidation of requirements allowing true portability across programs and platforms.

Finally, since the Tunable Loop™ offers a continuum of design flexibility, it offers a superior capability compared to other solutions where only a discrete set of pre-tuned settings are available. Just as voltage programming using an external resistor was once novel in the application of POL modules, the Tunable Loop’s programmability using an external resistor and capacitor is expected to become the standard in flexibility and optimization.