Subject: **Operation of the CPL Product Line Interface_Board**

Concept

The CPL_Interface_Board provides the hardware and firmware connectivity for demos and diagnostics purposes for CPL components. On one end of the board a 40-pin ribbon cable terminates the interface board the CPL shelf. On the other end the interface board provides inputs to two i^2C lines and one RS485 line. Communications interfaces are connected via one of these three connectors.

The board provides two 8-position dip switches for controlling the analog functions of the CPL system and a number of LEDs that display drive signals from the CPL system.

Power for the Interface_Board is derived from the +5V output of the power supply. The board is operational as soon as one of the power supplies receives AC power.

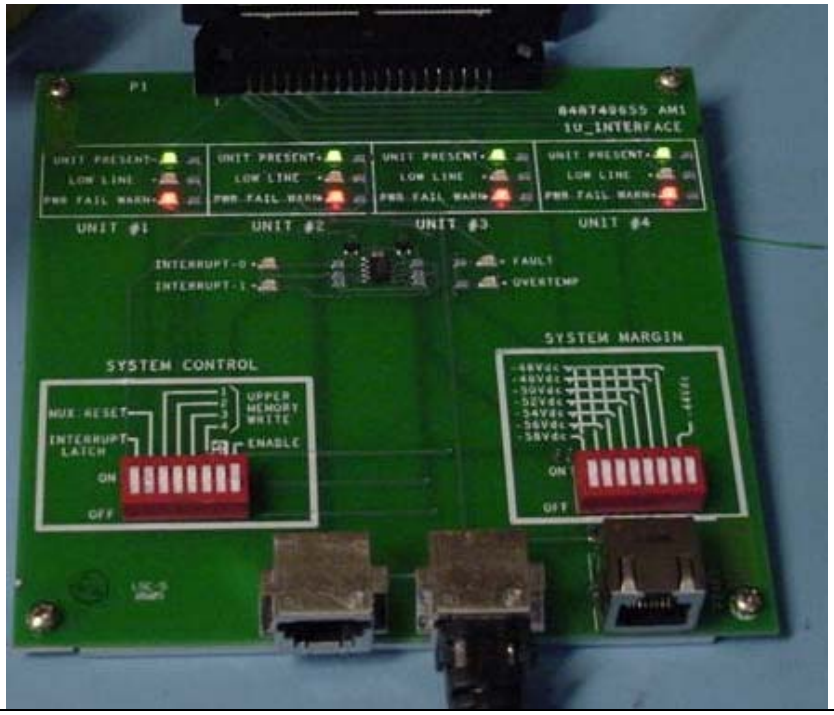


Figure 1: The CPL Interface Board

LED Annunciation

The top of the board shows four boxes, each one representing power supplies in the shelf under test. The three LEDs in each box are;

- **UNIT PRESENT** – This indicator is ON whenever power is present and at least one of the power supplies has AC power.

- **LOW LINE –** This indicator is ON when Input voltage is so low that the output power is lower than the power supply's full capacity rating.

  This condition is true when the input voltage is lower than 175Vac for High Line or when the input is below 135Vac for Low Line inputs of rectifiers.

- **PWR FAIL WARNING –** This indicator turns ON at least 5ms before the output would fall below regulation.

Below the four boxes are two sets of LEDs, and these are;

- **FAULT –** This indicator is ON when one or more of the power supplies issues a fault warning.

- **OVERTEMP –** This indicator is ON when one or more of the power supplies gets into an over-temperature warning or shutdown condition.

- **INTERRUPT-0 / INTERRUPT – 1** – These LEDs are functional with i^2C communications. The indicators are ON whenever the power supply requests service from the host controller. (See the *Technical Requirements PMBus Compliant Digital Interface for Rectifiers* for further information).

Dip Switch Operation

There are two independent dip switches, one for **System Control** and the other for **System margin.**

The **System Margin** dip switch manually changes the output voltage of the power supply from its 52Vdc factory setting. Switch 1 ON margins the power supply output to 58Vdc. Switches 1 and 2 ON margin the power supply output to 56Vdc and so on. Switch 8 margins the power supply output to 44Vdc whenever it is ON independent of the position of the other switches.

The **System Control** dip switch has the following functions;

- **INTERRUPT LATCH –** When set, the *Interrupt* LEDs stay ON. Turning this switch OFF would turn OFF the *Interrupt* LEDs as long as the *Interrupt* signal has extinguished.

- **MUX.RESET** – The CPL platform offers two independent, redundant, i^2C busses labeled i2C-0 and i2C-1. Selection of which bus the power supply will communicate with is accomplished by a Philips PCA9541 2-to-1 Master Selector. The PCA9541 is configured such that i2C-0 is active on power up. Changing the communications port is done by firmware. The PCA9541 also offers a RESET pin. In case of bus hang-up for any reason, RESET reconfigures the device into its initial state. In addition, the device issues a set of reset commands to the downstream devices as well. For additional information please consult the application notes and data sheet for the PCA9541.

- **UPPER MEMORY WRITE 1 – 4 –** Each of the four power supplies in the shelf contains an internal EEPROM. Turning these switches ON enables a *write* instruction into the upper ¼ of memory. Although this feature is available, it should be used with caution because a re-write will erase factory provided information. For further

information see the *PMBus Compliant Digital Interface* technical requirements document.

- **RS485 –** This bit configures the power supply into either the i^2C or the RS485 mode upon power up. If the switch is OFF, the power supply will power up in i^2C or analog mode. In this mode the SYSTEM CONTROL switches and the two i^2C communications ports are active. If the switch is ON, the power supply will power up in RS485 mode. In RS485 mode the SYSTEM CONTROL switches are disabled and communications is switched to the RS485 connector.

  Please note that the power supply will remember its configuration setting as long as bias voltage is available to its internal DSP. If a power supply is removed from its slot, it should be unplugged for at least 30 seconds in order to discharge the internal bias voltage to the DSP. One visual clue to this discharge level is observing the spinning of the internal fans. If the fans stopped spinning then it is likely that internal Bias has discharged. This clue is not always conclusive because if AC power is not present when the power supply is unplugged then the fans did not spin in the first place. However, the power supply could have been back-biased by an adjacent power supply.

- **ENABLE –** This switch turns ON the interconnected system. Only one switch is required. The signal is cascaded to numerous shelves by the interconnecting cable set between shelves.

For communications set-up please consult the **Functional verification and debugging tool** applications note.

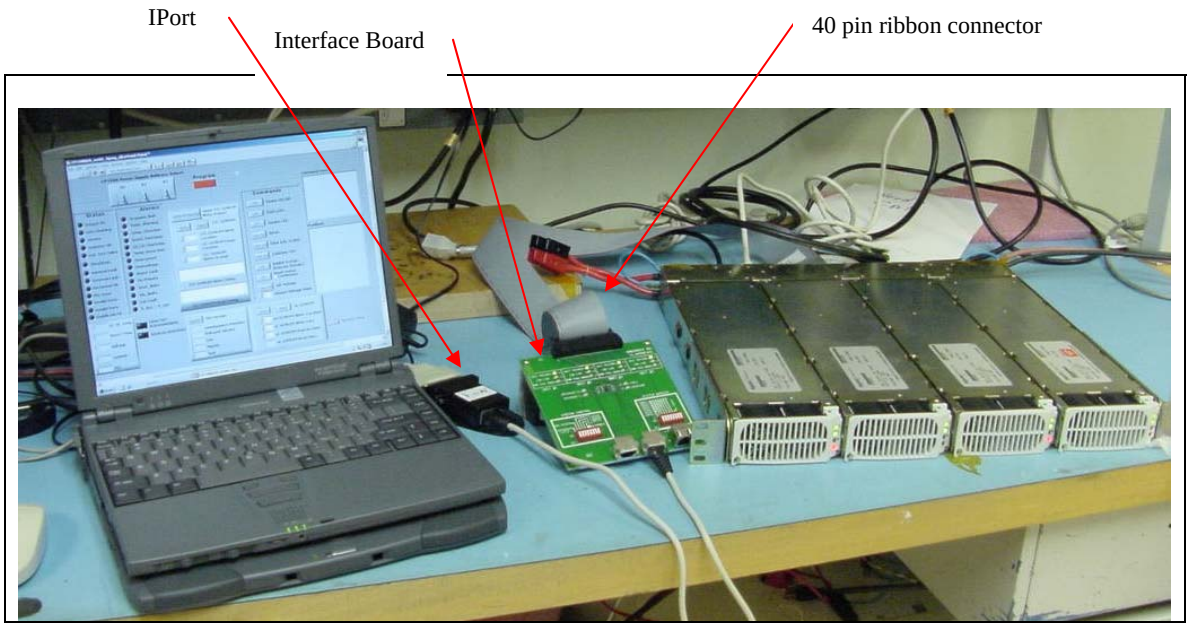
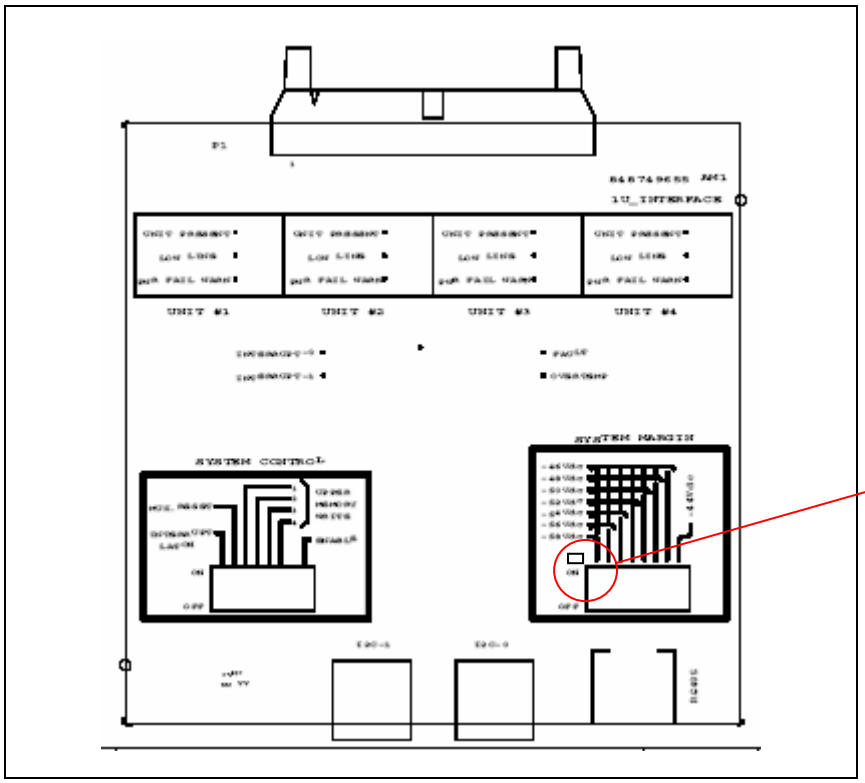


Figure 2: A complete communications system set-up

Errata

The first set of interface boards could have a component error on the board. The voltage divider network configuring margining includes a pull-up resistor to +5V on the interface board. This pull up resistor is already present inside the power supply. The pull-up resistor should be removed from the interface board in order for margining to configure the power supply to the voltage settings noted on the board stencil. With the pull-up present all the adjustment values have an offset resulting in a different voltage value set than noted on the board. Leaving the pull-up in place will not cause damage to the system.

The artwork below shows the location of this pull-up resistor.



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